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cont.

2. (Twice Amended) A ferroelectric memory, comprising:
a substrate;
a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the substrate;
a microstructure; and
a peripheral circuit for the passive matrix array, the peripheral circuit being separately formed on the microstructure, the microstructure being integrated on the substrate.

3. (Twice Amended) A ferroelectric memory, comprising:
a first microstructure;
a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the first microstructure;
a second microstructure;
a peripheral circuit for the passive matrix array, the peripheral circuit being separately formed on the second microstructure; and
a substrate, the first and second microstructures being integrated on the substrate.

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8. (Twice Amended) A ferroelectric memory, comprising:
a passive matrix array that includes memory cells formed of ferroelectric capacitors;
a peripheral circuit for the passive matrix array;
an associated circuit having a same or a different function as the memory cells;
a single substrate; and
a plurality of microstructures, the passive matrix array, the peripheral circuit and the associated circuit being separately formed on each of the plurality of microstructures, the microstructures being integrated on the single substrate.

9. (Twice Amended) A ferroelectric memory, comprising:
 a passive matrix array that includes memory cells formed of ferroelectric capacitors;
 a peripheral circuit for the passive matrix array; and
 a single microstructure, the passive matrix array and the peripheral circuit being separately fabricated and integrated on the single microstructure.

10. (Twice Amended) A ferroelectric memory, comprising:
 a first microstructure;
 a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the first microstructure;
 a second microstructure that is larger than the first microstructure, the first microstructure being provided in a part of the second microstructure to be integrated; and
 a peripheral circuit for the passive matrix array, the peripheral circuit being separately formed on the second microstructure.

12. (Twice Amended) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit for the passive matrix array, the method comprising:
 forming the passive matrix array on a microstructure;
 separately forming the peripheral circuit on a substrate; and
 integrating the microstructure on the substrate.

13. (Twice Amended) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit for the passive matrix array, the method comprising:
 forming the passive matrix array on a substrate;
 separately forming the peripheral circuit on a microstructure; and
 integrating the microstructure on the substrate.

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14. (Twice Amended) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit for the passive matrix array, the method comprising:

forming the passive matrix array on a first microstructure;

separately forming the peripheral circuit on a second microstructure; and

integrating the first and second microstructures on a substrate.

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18. (Twice Amended) A method of fabricating a ferroelectric memory, which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit for the passive matrix array, the method comprising:

forming the passive matrix array on a first microstructure;

separately forming the peripheral circuit on a second microstructure which is larger than the first microstructure; and

providing the first microstructure in a part of the second microstructure to be integrated.

19. (Twice Amended) A method of fabricating a ferroelectric memory, which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit for the passive matrix array, the method comprising:

separately forming the passive matrix array on each of a plurality of microstructures; and

providing the microstructures in layers to be integrated in a substrate.

REMARKS

Claims 1-25 are pending. Claims 7, 11 and 17 have been withdrawn from consideration. By this Amendment, claims 1-3, 8-10, 12-14, 18 and 19 are amended to indicate that the peripheral circuit is separately formed; and Figs. 24, 25 and 26A-26C are corrected by the attached Request for Approval of Drawing Corrections. Reconsideration based on the above amendments and following remarks is respectfully requested.